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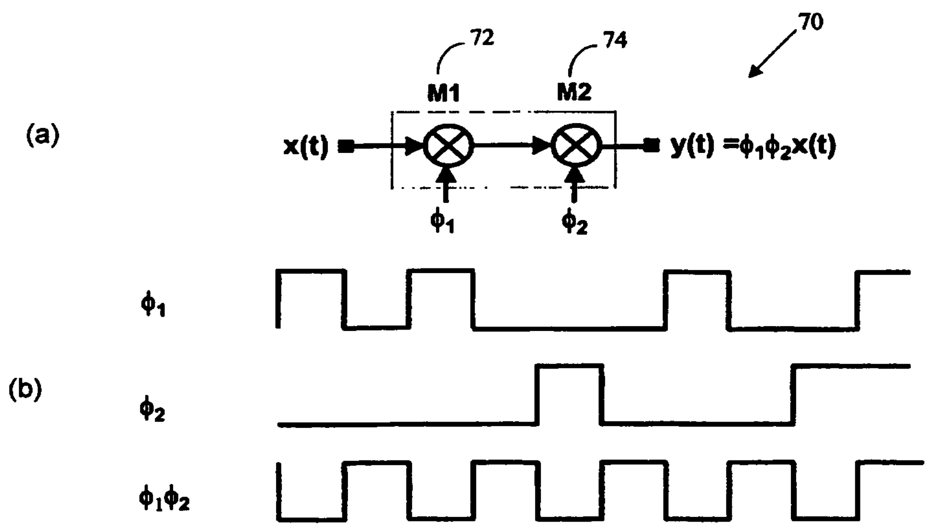
(54) Title: IMPROVED METHOD AND APPARATUS FOR DOWN-CONVERSION OF RADIO FREQUENCY (RF) SIGNALS



(57) Abstract: This patent describes a method of removing the LO-leakage and 1/f noise problems associated with direct conversion RF receivers and other demodulators. In order to solve this problem a virtual LO™ signal is generated within the RF signal path which is tuned to the incoming RF signal. The virtual local oscillator (VLO) signal is constructed using signals that do not contain a significant amount of power (or no power at all) at the LO frequency. Any errors in generating the virtual LO signal are minimized using a closed loop correction scheme.

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Improved Method and Apparatus for Down-Conversion of Radio Frequency (RF) Signals

The present invention relates generally to communications, and more specifically, to a fully-integrable method and apparatus for down conversion of radio frequency (RF) signals with reduced local oscillator (LO) leakage and 1/f noise.

Background of the Invention

Many communication systems modulate electromagnetic signals to higher frequencies for transmission, and subsequently demodulate those high frequencies back to their original frequency band when they reach the receiver. The original (or baseband) signal, may be, for example: data, voice or video. These baseband signals may be produced by transducers such as microphones or video cameras, be computer generated, or transferred from an electronic storage device.

All of these signals are generally referred to as radio frequency (RF) signals, which are electromagnetic signals, that is, waveforms with electrical and magnetic properties within the electromagnetic spectrum normally associated with radio wave propagation. The electromagnetic spectrum was traditionally divided into 26 alphabetically designated bands, however, the ITU formally recognizes 12 bands, from 30 Hz to 3000 GHz. New bands, from 3 THz to 3000 THz, are under active consideration for recognition.

Wired communication systems which employ such modulation and demodulation techniques include computer communication systems such as local area networks (LANs), point to point signalling, and wide area networks (WANs) such as the Internet. These networks generally communication data signals over electrical or optical fibre chanels. Wireless communication systems which may employ modulation and demodulation include those for public broadcasting such as AM and FM radio, and UHF and VHF television. Private communication systems may include cellular telephone networks, personal paging devices, HF radio systems used by taxi services, microwave backbone networks, interconnected appliances under the Bluetooth standard, and satellite communications. Other wired and wireless systems which use RF modulation and demodulation would be known to those skilled in the art.

One of the current problems in the art, is to develop physically small and inexpensive modulation and demodulation techniques and devices that have good

performance characteristics. For cellular telephones, for example, it is desirable to have a receiver which can be fully integrated onto an integrated circuit.

Several attempts have been made at completely integrating communication receiver designs, but have met with limited degrees of success. Most RF receivers use the "super-heterodyne" topology, which provides good performance, but does not meet the desired level of integration for modern wireless systems. The super-heterodyne topology typically requires at least two high quality filters that cannot be economically integrated within any modern IC technology. Other RF receiver topologies exist, such as image rejection architectures, which can be completely integrated on a chip but lack in overall performance.

Existing solutions and their associated problems and limitations are summarized below:

1. Super-heterodyne:

The super-heterodyne receiver uses a two-step frequency translation method to convert an RF signal to a baseband signal. **Figure 1** presents a block diagram of a typical super-heterodyne receiver **10**. The mixers labelled M1 **12**, MI **14**, and MQ **16** are used to translate the RF signal to baseband or to some intermediate frequency (IF). The balance of the components amplify the signal being processed and filter noise from it.

The RF band pass filter (BPF1) **18** first filters the signal coming from the antenna **20** (note that this band pass filter **18** may also be a duplexer). A low noise amplifier **22** then amplifies the filtered antenna signal, increasing the strength of the RF signal and reducing the noise figure of the receiver **10**. The signal is next filtered by another band pass filter (BPF2) **24** usually identified as an image rejection filter. The signal then enters mixer M1 **12** which multiplies the signal from the image rejection filter **24** with a periodic signal generated by the local oscillator (LO1) **26**. The mixer M1 **12** receives the signal from the image rejection filter **24** and translates it to a lower frequency, known as the first intermediate frequency (IF1).

Generally, a mixer is a circuit or device that accepts as its input two different frequencies and presents at its output:

(a) a signal equal in frequency to the sum of the frequencies of the input signals;

(b) a signal equal in frequency to the difference between the frequencies of the input signals; and

(c) the original input frequencies.

The typical embodiment of a mixer is a digital switch which may have significantly more tones than stated above.

The IF1 signal is next filtered by a band pass filter (BPF3) **28** typically called the channel filter, which is centred around the IF1 frequency, thus filtering out mixer signals (a) and (c) above.

The signal is then amplified by an amplifier (IFA) **30**, and is split into its in-phase (I) and quadrature (Q) components, using mixers MI **14** and MQ **16**, and orthogonal signals generated by local oscillator (LO2) **32** and 90 degree phase shifter **34**. LO2 **32** generates a periodic signal which is typically tuned the IF1 frequency. The signals coming from the outputs of MI **14** and MQ **16** are now at baseband, that is, the frequency at which they were originally generated. The two signals are next filtered using low pass filters LPFI **36** and LPFQ **38** to remove the unwanted products of the mixing process, producing baseband I and Q signals. The signals may then be amplified by gain-controlled amplifiers AGCI **40** and AGCQ **42**, and digitized via analog to digital converters ADI **44** and ADQ **46** if required by the receiver.

The main problems with the super-heterodyne design are:

- it requires expensive off-chip components, particularly band pass filters **18**, **24**, **28**, and low pass filters **36**, **38**;
- the off-chip components require design trade-offs that increase power consumption and reduce system gain;
- image rejection is limited by the off-chip components, not by the target integration technology;
- isolation from digital noise can be a problem; and
- it is not fully integratable.

2. Direct Conversion:

Direct conversion architectures demodulate RF signals to baseband in a single step, by mixing the RF signal with a local oscillator signal at the carrier frequency. There is therefore no image frequency, and no image components to corrupt the signal. Direct conversion receivers offer a high level of integratability, but also have several important problems. Hence, direct conversion receivers have thus far proved useful only for signalling formats that do not place appreciable signal energy near DC after conversion to baseband.

A typical direct conversion receiver is shown in **Figure 2**. The RF band pass filter (BPF1) **18** first filters the signal coming from the antenna **20** (this band pass

filter **18** may also be a duplexer). A low noise amplifier **22** is then used to amplify the filtered antenna signal, increasing the strength of the RF signal and reducing the noise figure of the receiver **10**.

The signal is then split into its quadrature components using mixers MI **14** and MQ **16**, and orthogonal signals generated by local oscillator (LO2) **32** and 90 degree phase shifter **34**. LO2 **32** generates a periodic signal which is tuned the incoming wanted frequency rather than an IF frequency as in the case of the super-heterodyne receiver. The signals coming from the outputs of MI **14** and MQ **16** are now at baseband, that is, the frequency at which they were originally generated. The two signals are next filtered using low pass filters LPFI **36** and LPFQ **38**, are amplified by gain-controlled amplifiers AGCI **40** and AGCQ **42**, and are digitized via analog to digital converters ADI **44** and ADQ **46**.

Direct conversion RF receivers have several advantages over super-heterodyne systems in term of cost, power, and level of integration, however, there are also several serious problems with direct conversion. These problems include:

- noise near baseband (that is, 1/f noise) which corrupts the desired signal;
- local oscillator (LO) leakage in the RF path that creates DC offsets. As the LO frequency is the same as the incoming signal being demodulated, any leakage of the LO signal onto the antenna side of the mixer will pass through to the output side as well;
- local oscillator leakage into the RF path that causes desensitization. Desensitation is the reduction of desired signal gain as a result of receiver reaction to an undesired signal. The gain reduction is generally due to overload of some portion of the receiver, such as the AGC circuitry, resulting in suppression of the desired signal because the receiver will no longer respond linearly to incremental changes in input voltage.
- noise inherent to mixed-signal integrated circuits corrupts the desired signal;
- large on-chip capacitors are required to remove unwanted noise and signal energy near DC, which makes integrability expensive. These capacitors are typically placed between the mixers and the low pass filters; and
- errors are generated in the quadrature signals due to inaccuracies in the 90 degree phase shifter.

3. Image Rejection Architectures:

Several image rejection architectures exist, the two most well known being the Hartley Image Rejection Architecture and the Weaver Image Rejection

Architecture. There are other designs, but they are generally based on these two architectures while some methods employ poly-phase filters to cancel image components. Generally, either accurate signal phase shifts or accurate generation of quadrature local oscillators are employed in these architectures to cancel the image frequencies. The amount of image cancellation is directly dependent upon the degree of accuracy in producing the phase shift or in producing the quadrature local oscillator signals.

Although the integratability of these architectures is high, their performance is relatively poor due to the required accuracy of the phase shifts and quadrature oscillators. This architecture has been used for dual mode receivers on a single chip.

4. Near Zero-IF Conversion:

This receiver architecture is similar to the direct conversion architecture, in that the RF band is brought close to baseband in a single step. However, the desired signal is not brought exactly to baseband and therefore DC offsets and 1/f noise do not contaminate the signal. Image frequencies are again a problem as in the super-heterodyne structure.

Additional problems encountered with near zero-IF architectures include:

- the need for very accurate quadrature local oscillators; and
- the need for several balanced signal paths for purposes of image cancellation.

5. Sub-sampling Downconversion:

This method of signal downconversion utilizes subsampling of the RF signal to cause the frequency translation. Although the level of integration possible with this technique is the highest among those discussed thus far, the subsampling downconversion method suffers from two major drawbacks:

- subsampling of the RF signal causes aliasing of unwanted noise power to DC. Sampling by a factor of m increases the downconverted noise power of the sampling circuit by a factor of $2m$; and
- subsampling also increases the effect of noise in the sampling clock. In fact, the clock phase noise power is increased by m^2 for sampling by a factor of m.

There is therefore a need for a method and apparatus of demodulating RF signals which allows the desired integrability along with good performance.

Summary of the Invention

It is therefore an object of the invention to provide a novel method and system of modulation which obviates or mitigates at least one of the disadvantages of the prior art.

One aspect of the invention is broadly defined as a radio frequency (RF) down-convertor with reduced local oscillator leakage, for demodulating an input signal *x(t)*, comprising: a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of the local oscillator signal being emulated; a first mixer coupled to the synthesizer for mixing the input signal *x(t)* with the time-varying signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and a second mixer coupled to the synthesizer and to the output of the first mixer for mixing the signal $x(t)\ \varphi_1$ with the time-varying signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

Brief Description of the Drawings

These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings in which:

Figure 1 presents a block diagram of a super-heterodyne system as known in the art;

Figure 2 presents a block diagram of a direct conversion or homodyne system as known in the art;

Figure 3 (a) presents a block diagram of a broad implementation of the invention;

Figure 3 (b) presents exemplary mixer input signals functions φ_1 and φ_2 plotted in amplitude against time;

Figure 4 presents a block diagram of quadrature demodulation in an embodiment of the invention;

Figure 5 presents a block diagram of an embodiment of the invention employing error correction by measuring the amount of power at baseband;

Figure 6 presents a block diagram of a receiver in a preferred embodiment of the invention;

Figure 7 presents a block diagram of an embodiment of the invention employing a filter placed between mixers M1 and M2; and

Figure 8 presents a block diagram of an embodiment of the invention employing N mixers and N mixing signals.

Detailed Description of Preferred Embodiments of the Invention

A device which addresses the objects outlined above, is presented as a block diagram in **Figure 3(a)**. This figure presents a demodulator topography **70** in which an input signal *x(t)* is mixed with signals which are irregular in the time domain (TD), which effect the desired demodulation. A virtual local oscillator (VLO) is generated by multiplying two functions (labelled φ_1 and φ_2) within the signal path of the input signal *x(t)* using two mixers M1 **72** and M2 **74**. The mixers described within this invention would have the typical properties of mixers within the art, that is, they would have an associated noise figure, linearity response, and conversion gain. The selection and design of these mixers would follow the standards known in the art, and could be, for example, double balanced mixers. Though this figure implies various elements are implemented in analogue form they can be implemented in digital form.

The two time-varying functions φ_1 and φ_2 that comprise the virtual local oscillator (VLO) signal have the property that their product is equal to the local oscillator (LO) being emulated, however, neither of the two signals has a significant level of power at the frequency of the local oscillator being emulated. As a result, the desired demodulation is affected, but there is no LO signal to leak in the RF path. **Figure 3b** depicts possible functions for φ_1 and φ_2 .

To minimize the leakage of LO power into the RF signal, as in the case of direct conversion receivers, the preferred criteria for selecting the functions φ_1 and φ_2 are:

(i) that φ_1 and φ_2 do not have any significant amount of power at the carrier frequency. That is, the amount of power generated at the carrier frequency should not effect the overall system performance of the receiver in a significant manner;

(ii) the signals required to generate φ_1 and φ_2 should not have a significant amount of power at the RF carrier frequency; and

(iii) if x(t) is an RF signal, φ_1 φ_1 φ_2 should not have a significant amount of power within the bandwidth of the RF signal at baseband.

Conditions (i) and (ii) ensure an insignificant amount of power is generated within the system at the carrier frequencies which would cause an equivalent LO

leakage problem found in conventional direct conversion topologies. Condition (iii) ensures that if φ_1 leaks into the input port, it does not produce a signal within the baseband signal at the output.

Various functions can satisfy the conditions provided above, several of which are described hereinafter, however it would be clear to one skilled in the art that other similar pairs of signals may also be generated. These signals can in general be random, pseudo-random, periodic functions of time, or digital waveforms. As well, rather than employing two signals as shown above, sets of three or more may be used (additional description of this is given hereinafter).

It would also be clear to one skilled in the art that TD signals may be generated which provide the benefits of the invention to greater or lesser degrees. While it is possible in certain circumstances to have almost no leakage, it may be acceptable in other circumstances to incorporate virtual LO signals which still allow a degree of LO leakage.

It is also important to note that in order to reduce the 1/f noise commonly found in direct conversion receivers, the significant frequency components of φ_2 should be at a lower frequency than the frequency components of the function φ_1.

The topology of the invention is similar to that of direct conversion, but provides a fundamental advantage: minimal leakage of a local oscillator (LO) signal into the RF band. The topology also provides technical advantages over dual conversion topologies such as super-heterodyne systems:

- removes the necessity of having a second LO and various filters; and
- has a higher level of integration as the components it does require are easily placed on an integrated circuit.

While the basic implementation of the invention may produce errors in generating the virtual local oscillator (VLO), solutions to this problem are available and are described hereinafter.

The invention provides the basis for a fully integrated communications receiver. Increasing levels of integration have been the driving impetus towards lower cost, higher volume, higher reliability and lower power consumer electronics since the inception of the integrated circuit. This invention will enable communications receivers to follow the same integration route that other consumer electronic products have benefited from.

Specifically, advantages from the perspective of the manufacturers when incorporating the invention into a product include:

1. significant cost savings due to the decreased parts count of an integral device. Decreasing the parts count reduces the cost of inventory control, reduces the costs associated with warehousing components, and reduces the amount of manpower to deal with higher part counts;
2. significant cost savings due to the decreased manufacturing complexity. Reducing the complexity reduces time to market, cost of equipment to manufacture the product, cost of testing and correcting defects, and reduces time delays due to errors and problems on the assembly line;
3. reduces design costs due to the simplified architecture. The simplified architecture will shorten the first-pass design time and total design cycle time as a simplified design will reduce the number of design iterations required;
4. significant space savings and increased manufacturability due to the high integrability and resulting reduction in product form factor (physical size). This implies huge savings throughout the manufacturing process as smaller device footprints enable manufacturing of products with less material such as printed circuit substrate, smaller product casing and smaller final product packaging;
5. simplification and integrability of the invention will yield products with higher reliability, greater yield, less complexity, higher life span and greater robustness;
6. due to the aforementioned cost savings, the invention will enable the creation of products that would otherwise be economically unfeasible;

Hence, the invention provides the manufacturer with a significant competitive advantage.

From the perspective of the consumer, the marketable advantages of the invention include:

1. lower cost products, due to the lower cost of manufacturing;
2. higher reliability as higher integration levels and lower parts counts imply products will be less prone to damage from shock, vibration and mechanical stress;
3. higher integration levels and lower parts counts imply longer product life span;
4. lower power requirements and therefore lower operating costs;

5. higher integration levels and lower parts counts imply lighter weight products;
6. higher integration levels and lower parts counts imply physically smaller products; and
7. the creation of economical new products.

The present invention relates to the translation of an RF signal directly to baseband and is particular concerned with solving the LO-leakage problem and the 1/f noise problems associated with the present art. The invention allows one to fully integrate a RF receiver on a single chip without using external filters. Furthermore the RF receiver can be used as a multi-standard receiver. Descriptions of such exemplary embodiments follow.

In many modulation schemes, it is necessary to demodulate both I and Q components of the input signal, which requires a demodulator **80** as presented in the block diagram of **Figure 4**. In this case, four demodulation functions would have to be generated: φ_{1I} which is 90 degrees out of phase with φ_{1Q}; and φ_{2I} which is 90 degrees out of phase with φ_{2Q}. The pairing of φ_{1I} and φ_{2I} must meet the function selection criteria listed above, as must the pairing of φ_{1Q} and φ_{2Q}. The mixers **82, 84, 86, 88** are standard mixers as known in the art.

As shown in **Figure 4**, mixer M1I **82** receives the input signal *x(t)* and demodulates it with φ_{1I}; subsequent to this, mixer M2I **84** demodulates signal *x(t)* φ_{1I} with φ_{2I} to yield the in-phase component of the input signal at baseband, that is, *x(t)* $\varphi_{1I}\varphi_{2I}$. A complementary process occurs on the quadrature side of the demodulator, where mixer M1Q **86** receives the input signal *x(t)* and demodulates it with φ_{1Q}; after which mixer M2Q **88** demodulates signal *x(t)* φ_{1Q} with φ_{2Q} to yield the quadrature phase component of the input signal at baseband, that is, *x(t)* $\varphi_{1Q}\varphi_{2Q}$. Generation of appropriate φ_{1I}, φ_{2I}, φ_{1Q} and φ_{2Q} signals would be clear to one skilled in the art from the teachings herein.

In the analysis above timing errors that would arise when constructing the *VLO* have been neglected (timing errors can be in the form of a delay or a mismatch in rise/fall times. In the analysis which follows, only delays are considered, but the same analysis can be applied to rise/fall times. The actual *VLO* that is generated can be written as:

$$VLO_a = VLO_i + \varepsilon_{VLO}(t) \qquad (1)$$

where VLO_a is the actual VLO generated, VLO_i is the ideal VLO without any timing error, and $\varepsilon_{VLO}(t)$ absorbs the error due to timing errors. Therefore, the output signal of the virtual LO topology, denoted as y(t), becomes:

$$y(t) = x(t) \times [VLO_i + \varepsilon_{VLO}(t)] \qquad (2)$$

The term $x(t)\ VLOi$ is the wanted term and $x(t)\ \varepsilon_{VLO}(t)$ is a term that produces aliasing power into the wanted signal. The term $\varepsilon_{VLO}(t)$ can also be thought of a term that raises the noise floor of the VLO. This term would produce in-band aliasing with power in the order of $\overline{\varepsilon_{VLO}}^2$, which is directly related to the bandwidth of the RF signal divided by the unity current gain frequency of the IC technology it is implemented in; assuming the worst-case scenario. This may be a serious problem for some applications. However, by selecting φ_1 and φ_2 carefully and by placing an appropriate filter at the input of the structure, the amount of aliasing power can be reduced significantly, though it can never be completely eliminated due to timing errors.

There are several ways one could further reduce the amount of aliasing power, for example, by using a closed loop configuration as described below. The term $x(t)\ \varepsilon_{VLO}(t)$ contains two terms at baseband:

(i) aliasing power P_a, and

(ii) power of the wanted signal, but at a reduced power level which is on the order of delay error $P_{w\varepsilon}$.

Therefore, the total power at base-band (denoted by P_M) can be decomposed into three components:

(i) the power of the wanted signal, P_w,

(ii) the power of the aliasing terms, P_a, and

(iii) the power of the wanted signal arising from the term, $P_{w\varepsilon}$ (this power can either be positive or negative). Therefore,

$$P_M = P_w + P_{w\varepsilon}(\tau) + P_a(\tau) \qquad (3)$$

Note that $P_{w\varepsilon}$ and P_a are a function of the delay τ. Since $|P_w| >> |P_{w\varepsilon}|$, (3) becomes,

$$P_M = P_w + P_a(\tau) \qquad (4)$$

If the power, P_M is measured and τ is adjusted in time, one can reduce the term Pa to zero (or close to zero). Mathematically this can be done if the slope of P_M with the delay τ is set to zero; that is:

$$\frac{dP_M}{d\tau} = \frac{dP_a(\tau)}{d\tau} = 0 \qquad (5)$$

A system diagram of this procedure is illustrated in **Figure 5** (a more detailed description is provided in the paragraph below). The power measurement scheme and the element blocks required to detect when $\frac{dP_M}{d\tau} = 0$, can be implemented within a digital signal processing unit (DSP). Also illustrated in **Figure 5** is a visual representation of the power measured versus delay, which identifies an optimum point at which $\frac{dP_M}{d\tau} = 0$.

In the block diagram of **Figure 5** the RF signal is first multiplied by the signals φ_1 and φ_2 via mixers M1 **72** and M2 **74**, respectively. The signal is next filtered via a low pass filter (LPF) **102**, which is used to reduce the amount of out of band power, which may cause the subsequent elements to compress in gain or distort the wanted signal. The design of this LPF **102**, which may also be a band pass filter, depends on the bandwidth of the wanted signal.

Any DC offset is subsequently removed using a technique known in the art, such as a summer **104** and an appropriate DC offset source **105**. The signal is then filtered with LPF2 **106**, which provides further filtering of the base-band signal. The design of this filter depends on the system specifications and system design trade offs. The signal is then amplified using automatic gain control elements (AGC) **108** which provide a significant amount of gain to the filtered baseband signal. The design of AGC **108** depends on the system specifications and system design trade offs.

The physical order (that is, arrangement) of the two LPFs **102**, **106**, the DC offset correction **104**, and the gain control elements **108** can be rearranged to some degree. Such modifications would be clear to one skilled in the art.

The baseband signal power is then measured with power measurement unit **110**. The power is minimized with respect to the delay added onto the signal φ_2 by use of the $\frac{dP_M}{d(delay)} = 0$ detector **112**, and the delay controller **114** which manipulates the φ_2 source **116**. In general, the power can be minimized with respect to the rise time of φ_2 or a combination of delay and rise time. Furthermore, the power can be minimized with respect to the delay, rise time, or both delay and rise time of the signal φ_1, or both φ_1 and φ_2.

It would be clear to one skilled in the art that current or voltage may be measured rather than power in certain applications. As well, the phase delay of either or both of φ_1 and φ_2 may be modified to minimized the error.

It is preferred that this power measurement **110** and detection **112** be done within a digital signal processing unit (DSP) **118** after the baseband signal is digitized via an analog to digital converter, but it may be done with separate components, or analogue components.

Figure 6 presents a complete system block diagram of the preferred embodiment of the timing corrected apparatus of the invention **130**, handling in-phase and quadrature components of the input signal. Though the figure implies the use of analogue components, they can be implemented in digital form.

The front end which produces the filtered and amplified baseband signal is the same as that of **Figure 5**, except that two channels are used, one for in-phase and one for the quadrature component, as in **Figure 4**. Hence, components **132, 134, 136, 138, 140** and **142** of **Figure 6** correspond with components **72, 74, 102, 104, 106** and **108** of **Figure 5** respectively. The input signals to these components are slightly different, as the components of **Figure 6** are required to suit the in-phase component of the input signal. For example, the input to mixer **132** is a suitable in-phase φ_1I signal, such as that input to mixer M1I **82** of **Figure 4**, and the input to mixer **134** is a suitable in-phase signal φ_2I similar to that input to mixer M2I **84** of **Figure 4** which has been corrected for delay using the technique of **Figure 5**. A description of components for generating these two input signals follows hereinafter.

Two additional differences between the front end of the preferred embodiment of **Figure 6** and other embodiments described herein are:

- the generation of the DC offset signal for the summer **138** using the DSP **144** and a digital to analogue convertor (DAC) **150** (compare with the DC offset summer **104** and DC offset source **105** of **Figure 5**); and
- the addition of a third low pass filter LPF3I **146**, the de-aliasing filter for the analogue to digital convertor (ADC) **148** that follows. The design of this LPF3I **146** depends on the system specifications and design.

The design of the front end for the quadrature-phase of the input signal follows in the same manner, with components **152, 154, 156, 158, 160, 162, 164, 166** and **168** complementary to components **132, 134, 136, 138, 140, 142, 146, 148** and **150**, respectively. The input signals to these components are also quuadrature-phase complements to the in-phase signal inputs.

It is preferred to generate the inputs to the four mixers **132, 134, 152, 154** in the manner presented in **Figure 6**. Specifically, the $\varphi_1 I$ and $\varphi_1 Q$ generation block **170** generates signals $\varphi_1 I$ and $\varphi_1 Q$, while $\varphi_2 I$ and $\varphi_2 Q$ generation block **172** generates signals $\varphi_2 I$ and $\varphi_2 Q$. The input to these generation blocks **170, 172** is an oscillator which does not have a significant amount of signal power at the frequency of the RF signal. The construction of the necessary logic for these components would be clear to one skilled in the art from the description herein, and in particular, with reference to **Figure 3**. Such signals may be generated using basic logic gates, field programmable gate arrays (FPGA), read only memories (ROMs), micro-controllers or other devices known in the art. Further description and other means of generating such signals is presented in the co-pending patent application under the Patent Cooperation Treaty, Serial No. ____________.

Note that the outputs of the $\varphi_1 I$ and $\varphi_1 Q$ generation block **170** go directly to mixers **132** and **152**, and also to the clocking edge delay and correction block **174** which corrects the $\varphi_2 I$ and $\varphi_2 Q$ signals. The clocking edge delay and correction block **174** also receives I and Q output control signals from the DSP **144**, which are digitized by DAC **176** and **178**, and are time corrected at blocks **180** and **182**. Correction blocks **180** and **182** modify the digitized signals from DAC **176** and **178** as required to suit the clocking edge delay and correction block **174**. There also may be a connection between the $\varphi_1 I$ and $\varphi_1 Q$ generation block **170** and the $\varphi_2 I$ and $\varphi_2 Q$ generation block **172** which may be required where $\varphi_1 I$ and $\varphi_1 Q$ are generated

using signals $\varphi_2 I$ and $\varphi_2 Q$. Of course, this control line may also pass in the opposite direction.

In the exemplary system of **Figure 6**, the calculation of the power is done within the DSP unit and a correction signal is generated. The method for correcting the error in the LO signal has been described with respect to **Figure 5**.

One variation to the basic structure in **Figure 3a** is to add a filter **190** between the two mixers **72, 74** as shown in the block diagram of **Figure 7** to remove unwanted signals that are transferred to the output port. This filter **190** may be a low pass, high pass, or band pass filter depending on the receiver requirements. The filter **190** does not necessarily have to be a purely passive filter, that is, it can have active components.

Another variation is that several functions φ_1, φ_2, φ_3 ... φ_n may be used to generate the virtual LO, as presented in the block diagram of **Figure 8**. Here, φ_1* φ_2*... *φ_n has a significant power level at the LO frequency, but each of the functions φ_1... φ_n contain an insignificant power level at LO.

The electrical circuits of the invention may be described by computer software code in a simulation language, or hardware development language used to fabricate integrated circuits. This computer software code may be stored in a variety of formats on various electronic memory media including computer diskettes, CD-ROM, Random Access Memory (RAM) and Read Only Memory (ROM). As well, electronic signals representing such computer software code may also be transmitted via a communication network.

Clearly, such computer software code may also be integrated with the code of other programs, implemented as a core or subroutine by external program calls, or by other techniques known in the art.

The embodiments of the invention may be implemented on various families of integrated circuit technologies using digital signal processors (DSPs), microcontrollers, microprocessors, field programmable gate arrays (FPGAs), or discrete components. Such implementations would be clear to one skilled in the art.

The invention may be applied to various communication protocols and formats including: amplitude modulation (AM), frequency modulation (FM), frequency shift keying (FSK), phase shift keying (PSK), cellular telephone systems including analogue and digital systems such as code division multiple access (CDMA), time division multiple access (TDMA) and frequency division multiple access (FDMA).

The invention may be applied to such applications as wired communication systems include computer communication systems such as local area networks (LANs), point to point signalling, and wide area networks (WANs) such as the Internet, using electrical or optical fibre cable systems. As well, wireless communication systems may include those for public broadcasting such as AM and FM radio, and UHF and VHF television; or those for private communication such as cellular telephones, personal paging devices, wireless local loops, monitoring of homes by utility companies, cordless telephones including the digital cordless European telecommunication (DECT) standard, mobile radio systems, GSM and AMPS cellular telephones, microwave backbone networks, interconnected appliances under the Bluetooth standard, and satellite communications.

While particular embodiments of the present invention have been shown and described, it is clear that changes and modifications may be made to such embodiments without departing from the true scope and spirit of the invention.

WHAT IS CLAIMED IS:

1. A radio frequency (RF) down-convertor with reduced local oscillator leakage, for demodulating an input signal *x(t)*, comprising:

a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said time-varying signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal $x(t)\ \varphi_1$ with said time-varying signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

2. The radio frequency (RF) down-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said input signal *x(t)* at baseband.

3. The radio frequency (RF) down-convertor of claim 2, further comprising:

a DC offset correction circuit

4. The radio frequency (RF) down-convertor of claim 3, wherein said DC offset correction circuit comprises:

a DC source having a DC output; and

a summer for adding said DC output to an output of one of said mixers.

5. The radio frequency (RF) down-convertor of claim 2, further comprising:

a closed loop error correction circuit.

6. The radio frequency (RF) down-convertor of claim 5, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit and

a time-varying signal modification circuit for modifying a parameter of one of said time-varying signals to minimize said error level.

7. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a power measurement.

8. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a voltage measurement.

9. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a current measurement

10. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the phase delay of one of said time-varying signals.

11. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the fall or rise time of one of said time-varying signals.

12. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said time-varying signals.

13. The radio frequency (RF) down-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating time-varying signals φ_1 and φ_2, where said time-varying signals can change with time in order to reduce errors.

14. The radio frequency (RF) down-convertor of claim 1, further comprising:

a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

15. The radio frequency (RF) down-convertor of claim 2, wherein said time-varying signals are random.

16. The radio frequency (RF) down-convertor of claim 1, wherein said time-varying signals are pseudo-random.

17. The radio frequency (RF) down-convertor of claim 1, wherein said time-varying signals are irregular.

18. The radio frequency (RF) down-convertor of claim 1, wherein said time-varying signals are digital waveforms.

19. The radio frequency (RF) down-convertor of claim 1, wherein said time-varying signals are square waveforms.

20. The radio frequency (RF) down-convertor of claim 1, further comprising:
a local oscillator coupled to said synthesizer for providing a signal having a frequency that is an integral multiple of the desired mixing frequency.

21. A method of demodulating a radio frequency (RF) signal *x(t)* with reduced local oscillator leakage comprising the steps of:
generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;
mixing said input signal *x(t)* with said time-varying signal φ_1 to generate an output signal *x(t)* φ_1; and
mixing said signal *x(t)* φ_1 with said time-varying signal φ_2 to generate an output signal *x(t)* $\varphi_1 \varphi_2$.

22. An integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 20.

23. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 20.

24. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 20.

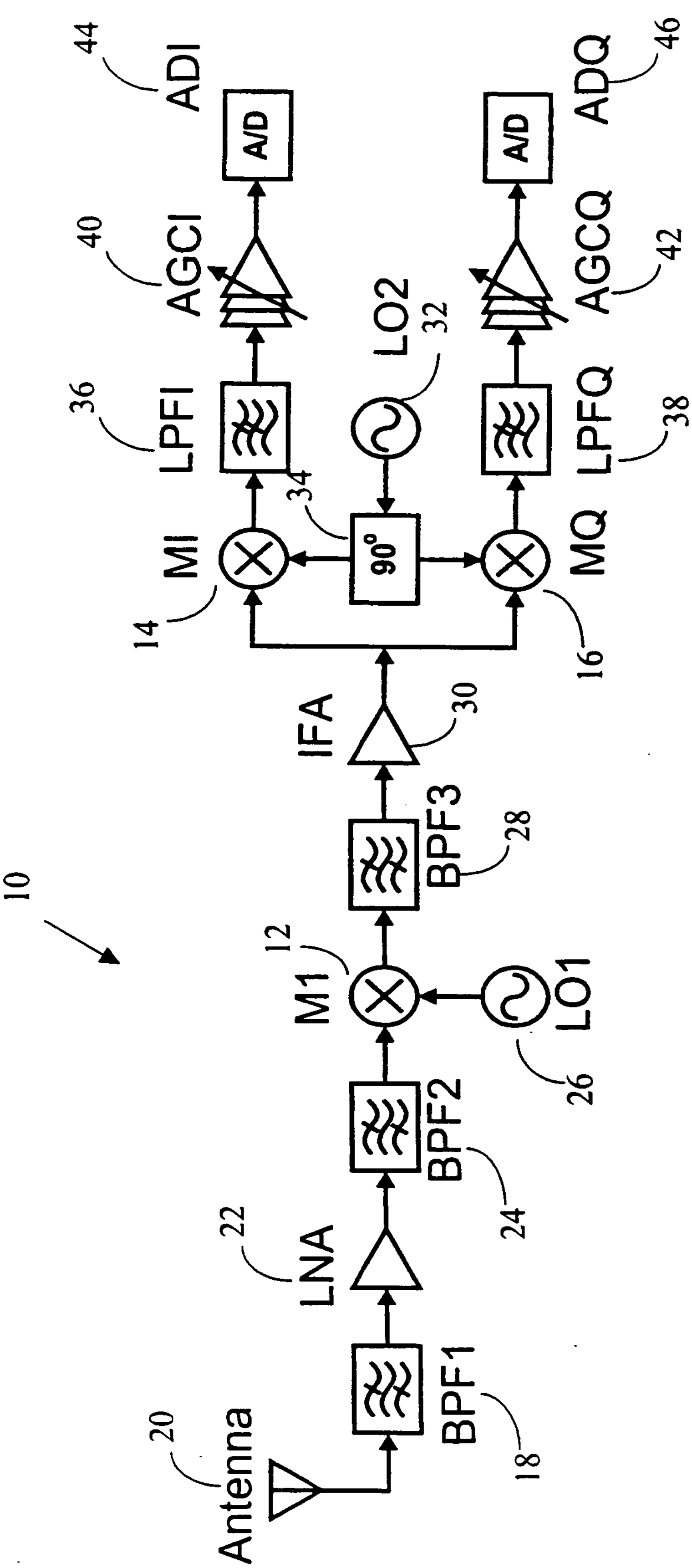

FIGURE 1 - PRIOR ART

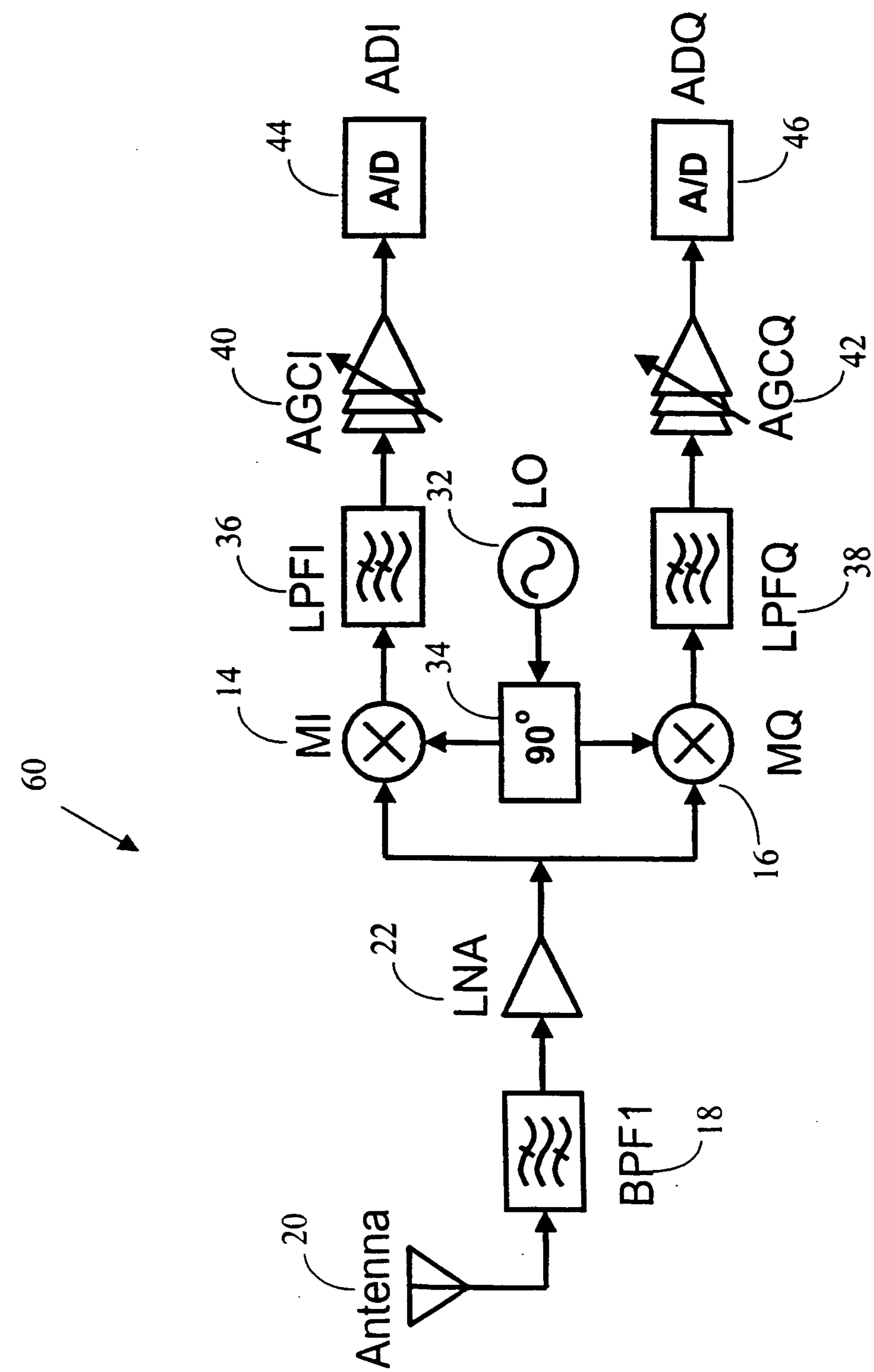

FIGURE 2 - PRIOR ART

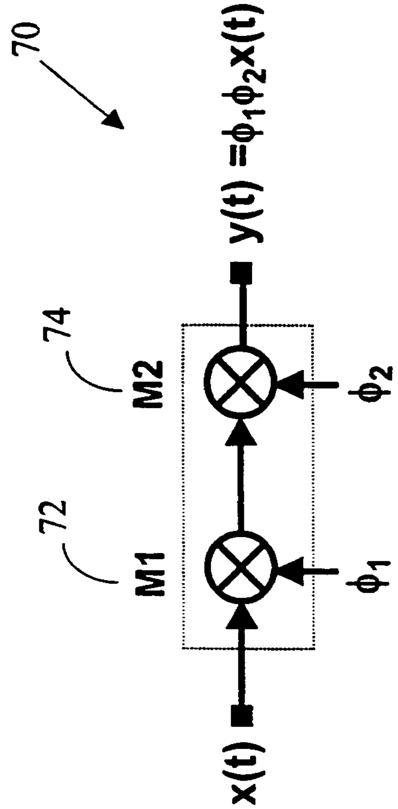

FIGURE 3(a)

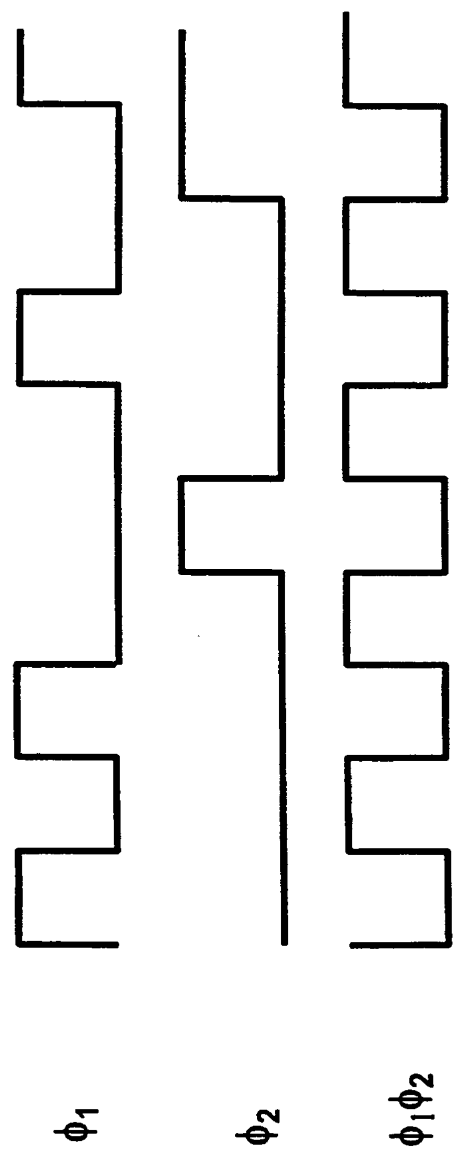

FIGURE 3(b)

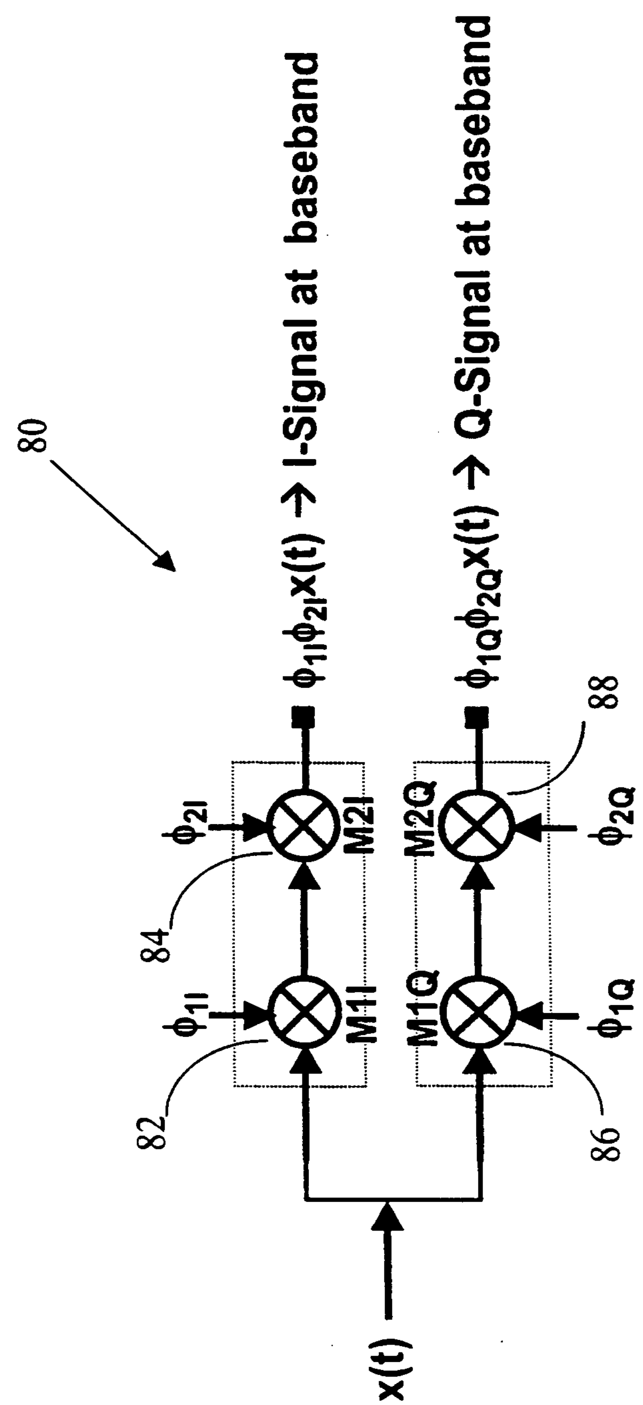
80
φ1Iφ2Ix(t) → I-Signal at baseband
φ1Qφ2Qx(t) → Q-Signal at baseband
φ2I
M2I
84
φ1I
M1I
82
M2Q
φ2Q
88
M1Q
φ1Q
86
x(t)

FIGURE 4

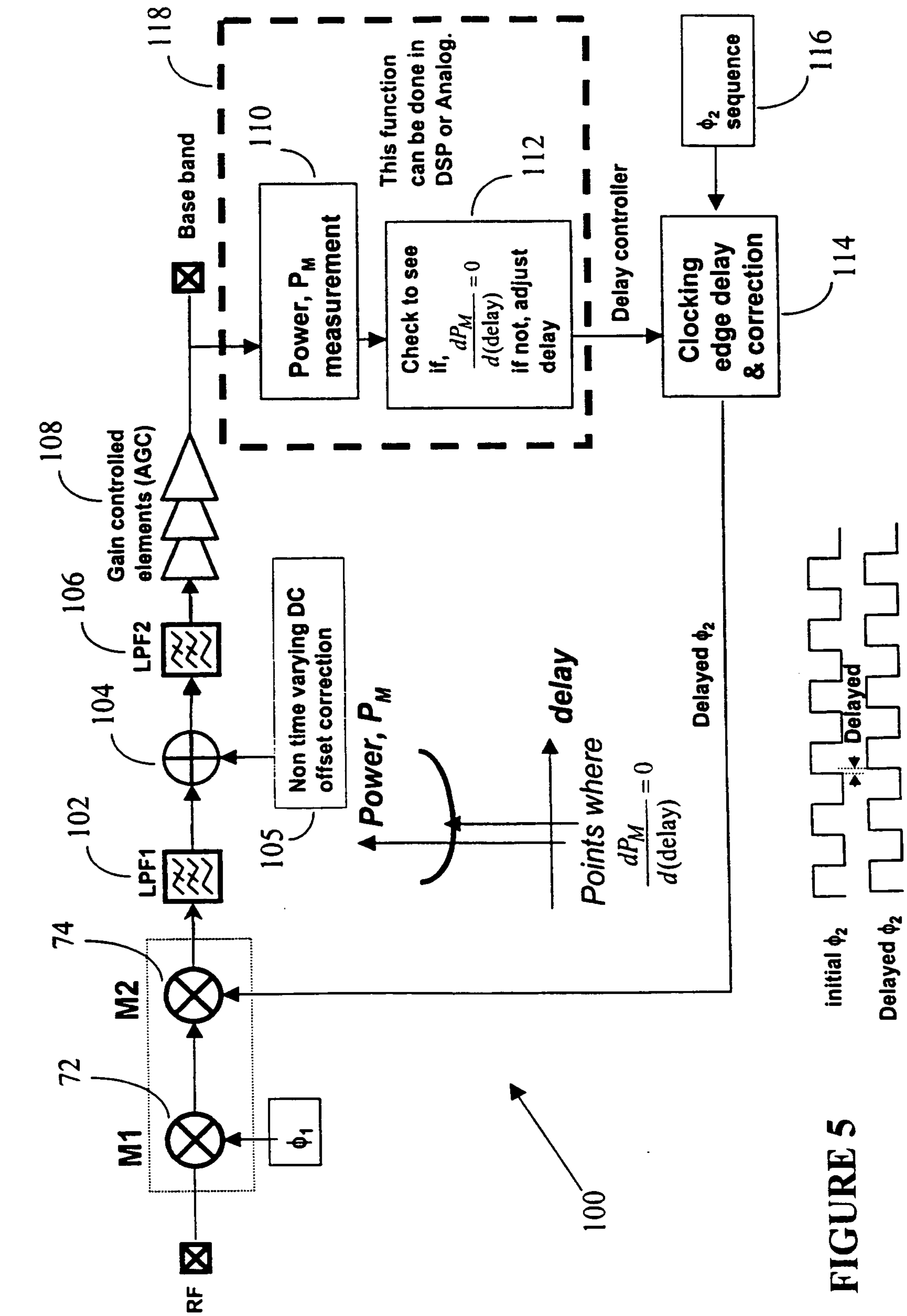
RF
M1
72
ϕ_1
M2
74
LPF1
102
104
Non time varying DC offset correction
105
LPF2
106
Gain controlled elements (AGC)
108
Base band
118
110
Power, P_M measurement
This function can be done in DSP or Analog.
112
Check to see if, $\frac{dP_M}{d(\text{delay})} = 0$ if not, adjust delay
Delay controller
Clocking edge delay & correction
114
ϕ_2 sequence
116
Delayed ϕ_2
Power, P_M
delay
Points where $\frac{dP_M}{d(\text{delay})} = 0$
Delayed
initial ϕ_2
Delayed ϕ_2
100

FIGURE 5

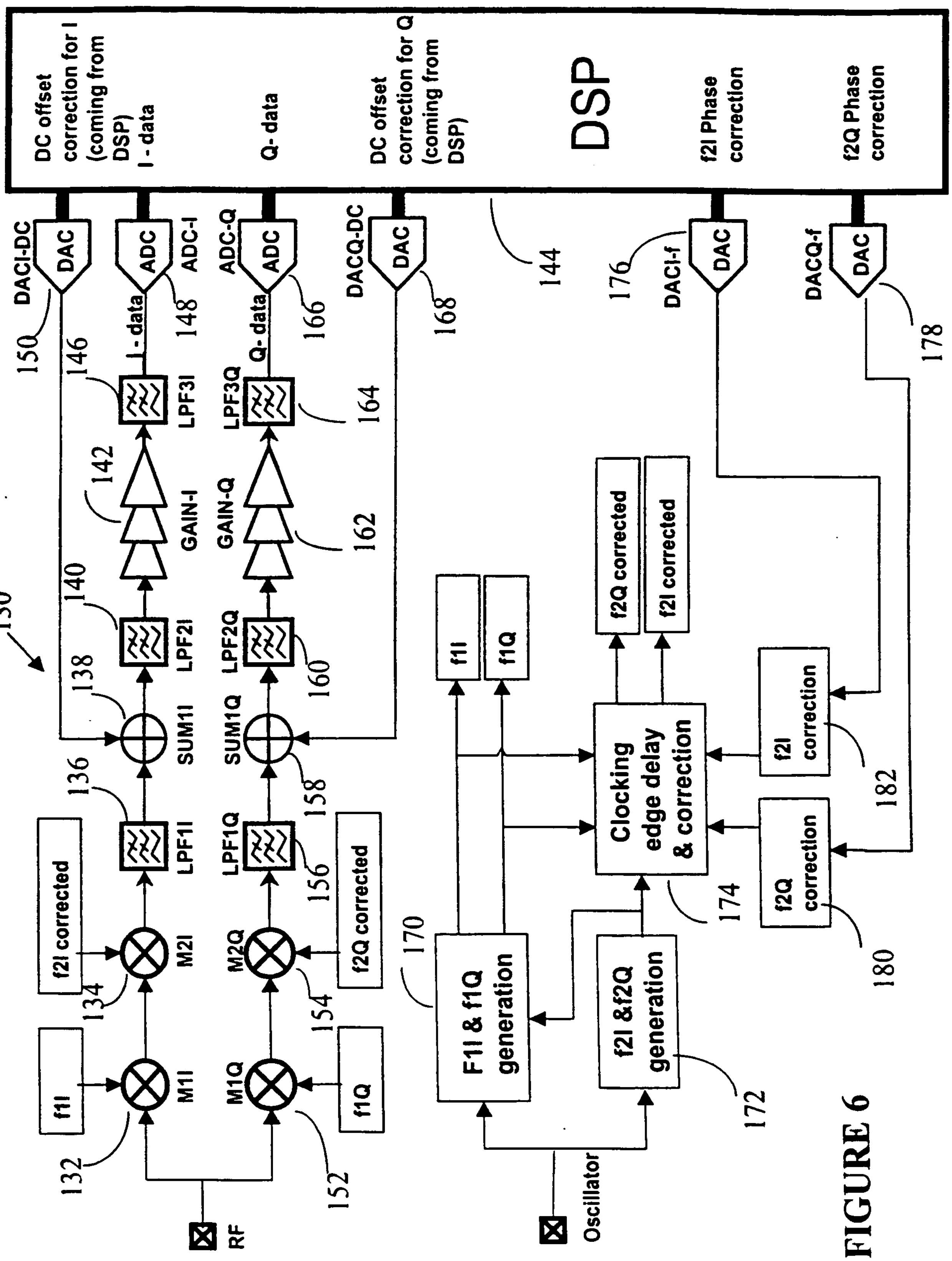
DSP
DC offset correction for I (coming from DSP)
I - data
Q- data
DC offset correction for Q (coming from DSP)
f2I Phase correction
f2Q Phase correction
DACI-DC
DAC
ADC
ADC-I
ADC-Q
DACQ-DC
DACI-f
DACQ-f
I - data
Q- data
LPF3I
LPF3Q
GAIN-I
GAIN-Q
LPF2I
LPF2Q
SUM1I
SUM1Q
LPF1I
LPF1Q
M2I
M2Q
M1I
M1Q
f1I
f1Q
f2I corrected
f2Q corrected
RF
Oscillator
F1I & f1Q generation
f2I &f2Q generation
Clocking edge delay & correction
f2I correction
f2Q correction
130
132
134
136
138
140
142
144
146
148
150
152
154
156
158
160
162
164
166
168
170
172
174
176
178
180
182

FIGURE 6

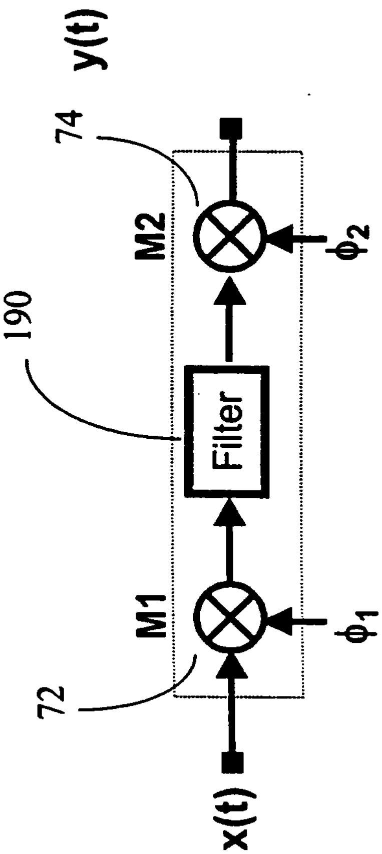

FIGURE 7

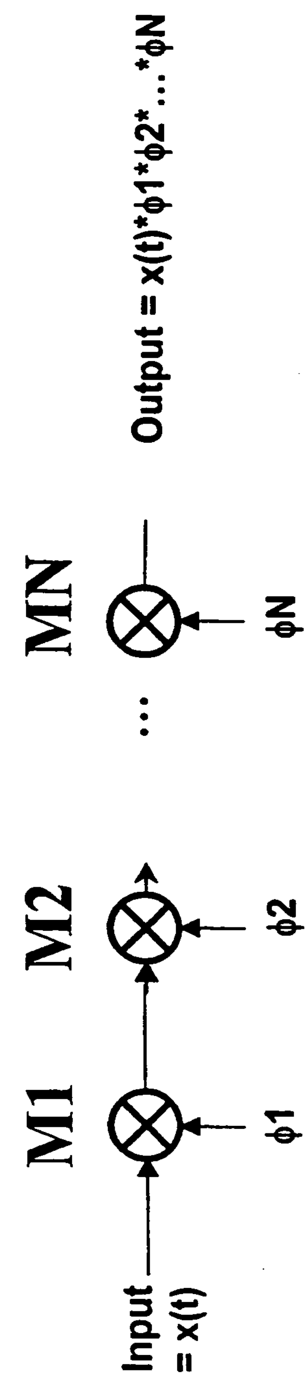

FIGURE 8

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(74) Agents: HARRIS, John, D. et al.; Gowling Lafleur Henderson LLP, Suite 2600, 160 Elgin Street, Ottawa, Ontario K1P 1C3 (CA).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

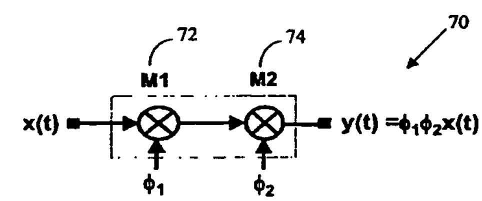
Published:
— *with international search report*

(88) Date of publication of the international search report: 26 July 2001

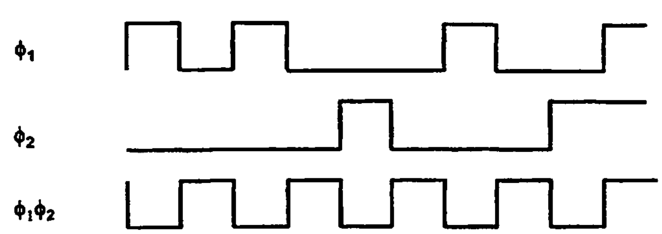
[Continued on next page]

(54) Title: FREQENCY TRANSLATOR USING A NON-PERIODIC LOCAL OSCILLATOR SIGNAL

(a)



(b)



(57) Abstract: This patent describes a method of removing the LO-leakage and 1/f noise problems associated with direct conversion RF receivers and other demodulators. In order to solve this problem a virtual LO™ signal is generated within the RF signal path which is tuned to the incoming RF signal. The virtual local oscillator (VLO) signal is constructed using signals that do not contain a significant amount of power (or no power at all) at the LO frequency. Any errors in generating the virtual LO signal are minimized using a closed loop correction scheme.

WO 01/17120 A3

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Two additional differences between the front end of the preferred embodiment of **Figure 6** and other embodiments described herein are:

- the generation of the DC offset signal for the summer **138** using the DSP **144** and a digital to analogue convertor (DAC) **150** (compare with the DC offset summer **104** and DC offset source **105** of **Figure 5**); and
- the addition of a third low pass filter LPF3I **146**, the de-aliasing filter for the analogue to digital convertor (ADC) **148** that follows. The design of this LPF3I **146** depends on the system specifications and design.

The design of the front end for the quadrature-phase of the input signal follows in the same manner, with components **152, 154, 156, 158, 160, 162, 164, 166** and **168** complementary to components **132, 134, 136, 138, 140, 142, 146, 148** and **150**, respectively. The input signals to these components are also quuadrature-phase complements to the in-phase signal inputs.

It is preferred to generate the inputs to the four mixers **132, 134, 152, 154** in the manner presented in **Figure 6**. Specifically, the φ_1I and φ_1Q generation block **170** generates signals φ_1I and φ_1Q, while φ_2I and φ_2Q generation block **172** generates signals φ_2I and φ_2Q. The input to these generation blocks **170, 172** is an oscillator which does not have a significant amount of signal power at the frequency of the RF signal. The construction of the necessary logic for these components would be clear to one skilled in the art from the description herein, and in particular, with reference to **Figure 3**. Such signals may be generated using basic logic gates, field programmable gate arrays (FPGA), read only memories (ROMs), micro-controllers or other devices known in the art. Further description and other means of generating such signals is presented in the co-pending patent application under the Patent Cooperation Treaty, Serial No. ____________.

Note that the outputs of the φ_1I and φ_1Q generation block **170** go directly to mixers **132** and **152**, and also to the clocking edge delay and correction block **174** which corrects the φ_2I and φ_2Q signals. The clocking edge delay and correction block **174** also receives I and Q output control signals from the DSP **144**, which are digitized by DAC **176** and **178**, and are time corrected at blocks **180** and **182**. Correction blocks **180** and **182** modify the digitized signals from DAC **176** and **178** as required to suit the clocking edge delay and correction block **174**. There also may be a connection between the φ_1I and φ_1Q generation block **170** and the φ_2I and φ_2Q generation block **172** which may be required where φ_1I and φ_1Q are generated

WHAT IS CLAIMED IS:

1. A radio frequency (RF) down-convertor with reduced local oscillator leakage, for demodulating an input signal *x(t)*, comprising:

a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said time-varying signal φ_1 to generate an output signal *x(t)* φ_1; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal *x(t)* φ_1 with said time-varying signal φ_2 to generate an output signal *x(t)* φ_1 φ_2.

2. The radio frequency (RF) down-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said input signal *x(t)* at baseband.

3. The radio frequency (RF) down-convertor of claim 2, further comprising:

a DC offset correction circuit

4. The radio frequency (RF) down-convertor of claim 3, wherein said DC offset correction circuit comprises:

a DC source having a DC output; and

a summer for adding said DC output to an output of one of said mixers.

5. The radio frequency (RF) down-convertor of claim 2, further comprising:

a closed loop error correction circuit.

6. The radio frequency (RF) down-convertor of claim 5, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit and

a time-varying signal modification circuit for modifying a parameter of one of said time-varying signals to minimize said error level.

7. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a power measurement.

8. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a voltage measurement.

9. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a current measurement

10. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the phase delay of one of said time-varying signals.

11. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the fall or rise time of one of said time-varying signals.

12. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said time-varying signals.

13. The radio frequency (RF) down-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating time-varying signals φ_1 and φ_2, where said time-varying signals can change with time in order to reduce errors.

14. The radio frequency (RF) down-convertor of claim 1, further comprising:

a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

15. The radio frequency (RF) down-convertor of claim 2, wherein said time-varying signals are random.

16. The radio frequency (RF) down-convertor of claim 1, wherein said time-varying signals are pseudo-random.

17. The radio frequency (RF) down-convertor of claim 1, wherein said time-varying signals are irregular.

18. The radio frequency (RF) down-convertor of claim 1, wherein said time-varying signals are digital waveforms.

19. The radio frequency (RF) down-convertor of claim 1, wherein said time-varying signals are square waveforms.

20. The radio frequency (RF) down-convertor of claim 1, further comprising:
a local oscillator coupled to said synthesizer for providing a signal having a frequency that is an integral multiple of the desired mixing frequency.

21. A method of demodulating a radio frequency (RF) signal *x(t)* with reduced local oscillator leakage comprising the steps of:
generating time-varying signals φ_1 and φ_2, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;
mixing said input signal *x(t)* with said time-varying signal φ_1 to generate an output signal *x(t)* φ_1; and
mixing said signal *x(t)* φ_1 with said time-varying signal φ_2 to generate an output signal *x(t)* φ_1 φ_2.

22. An integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 20.

23. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 20.

24. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 20.

IN THE EUROPEAN PATENT OFFICE

The International Preliminary Examining Authority

In The Matter of International (PCT) Patent Application:

Applicant	: **SiRiFIC Wireless Corporation; et al.**
Serial No.	: **PCT/CA00/00994**
Filing Date	: **September 1, 2000**
Title	: **Improved Method And Apparatus For Down-Conversion Of Radio Frequency (RF) Signals**
Our File	: **08887954WO**
Date	: **December 17, 2001**

European Patent Office
Erhardstrasse 27
D-80298 Munich
FEDERAL REPUBLIC OF GERMANY

Response to Written Opinion

Dear Sir:

In response to the Written Opinion dated July 17, 2001, kindly amend this application as follows:

In the Description:

Substitute the attached page 14, for the corresponding page 14 presently on file.

In the Claims:

Substitute the attached claims pages 17 - 20, containing amended claims 1 - 26 for the corresponding pages 17 - 19 presently on file.

REMARKS

The Applicant notes that claims 1 and 21 (the new claim 23) have been amended, replacing the wording "time-varying" with "varying irregularly over time". The basis for this wording is found in the specification, particularly at lines 5 - 10 of page 7. New claims 21 and 22 have also been added, the amended claim 21 having basis in the specification at line 22 of page 8, and amended claim 22 having basis in Figure 3(b) and page 8 of the description, at lines 4 - 9. Other small amendments have also been made to other claims.

A compare document identifying the amendments made to the claims, has been attached, deleted text being struck-through and new text being underlined. No new matter has been added by way of these amendments.

Page 14 of the specification has been amended to enter the serial no. of the co-pending patent application referred to in the subject patent application as originally filed.

Under item V. 2. of the Written Opinion, the Examiner rejected claim 1 as lacking novelty in view of the publication of patent application WO 96 01006 (the "Honeywell application"). The Applicant submits that the amended claim 1 is novel in view of the Honeywell application as the Honeywell application does not recite all of the relevant limitations of this claim. Before considering the limitations of claim 1, a review of the Honeywell application is necessary.

Firstly, it is important to understand the purpose of the Honeywell design - to reject "spurious" signals. The term "spurious" appears in the Abstract, each of the 21 claims, and repeatedly in the specification. "Spurious" signals are defined by Honeywell on page 1 at lines 26 - 32, and again on page 6 at lines 17 - 26 with respect to a specific example: when a 90MHz LO signal is used to demodulate a desired 80MHz signal, and there is a 100MHz "spurious" signal in the signal path, then both the desired signal and the spurious signal will demodulate to 10MHz. They explain that it is generally impossible to separate these two signals as they will overlap one another at 10MHz.

Honeywell proposes a two-stage mixing topology that demodulates the desired signal, but suppresses this spurious signal. They do this by using two local oscillators (LO) that one would see in a typical superheterodyne topology, except that the two LO signals are modulated with the same spread spectrum (SS) pattern before they mix with the input signal.

They argue that the desired 80MHz signal will be encoded by the first SS LO, and then decoded by the second. They also argue that the 100MHz will not be properly decoded by the second SS LO, so this signal would simply remain as noise at the output (lines 20 - 21 of page 6 read: "In other words, the desired signal is correctly spread in the bandwidth but the undesired signal is not." At lines 25 - 26 of page 6, Honeywell then notes: "... the desired signal may be recovered since it is spread differently from the undesired signal.")

Honeywell does not explain how or why this works, but they clearly argue that this topology will not modulate or demodulate all input signals - only the desired input signal. Note that the filter plays no part in this selection process, as in the example they present, the intermediate frequency (IF) of both the 80MHz and 100MHz inputs will be the same - 10MHz.

Looking now at the amended claim 1, we see the limitation at lines 4 - 5 that: "$\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being

emulated", and at lines 10 - 11 that the second mixer will "generate an output signal *x(t)* $\varphi_1\ \varphi_2$". Clearly, Honeywell is arguing that their modulation/demodulation topology does not satisfy either of these requirements, otherwise both the 80MHz and 100MHz signals would be demodulated equally, down to 1MHz at the output. That is:

- the claim requires the output to be equal to $x(t)\ \varphi_1\ \varphi_2$;
- given inputs of 80MHz and 100MHz, and SS LO signals of 90MHz of 9MHz, what is the output of the Honeywell topology?
- according to the Honeywell document, the 80MHz will be demodulated to 1MHz, but the 100MHz signal will not;
- however, if the output of the Honeywell topology was equal to $x(t)\ \varphi_1\ \varphi_2$, then it would demodulate both the 80MHz and 100MHz signals down to 1MHz, overlapping one another;
- it does not, thus, the Honeywell application does not anticipate the limitations of claim 1

Therefore, claim 1 is in compliance with the requirements of PCT Article 33(1), (2).

The Applicant also notes that because Honeywell is attempting to address a different problem than that of the invention (i.e. rejecting spurious input signals), that the skilled technician would not consider the Honeywell application in addressing the problems of the invention.

Also under item V. 2., the Examiner submitted that a typical superheterodyne topology also anticipates claim 1, as any LO signal produces a "time-varying" signal. While the Applicant feels that the meaning of the term "time-varying" is clear from a reading of the patent specification as a whole, he has amended this wording to "which vary irregularly over time", to make the distinction more clear. As noted above, this wording has basis in the specification at lines 5 - 10 of page 7.

The Applicant therefore asks that the Examiner withdraw this objection under PCT Article 33(1), (2).

Under item V. 3., the Examiner submitted that because claim 21 (the amended claim 23) generally corresponds to the same scope as claim 1, it similarly lacks novelty in view of reference D1. The Applicant notes that the same amendments and arguments noted above with respect to claim 1, apply equally to the amended claim 23. The Applicant therefore submits that the amended claim 23 is in compliance with the requirements of PCT Article 33(1), (2), and asks that the Examiner withdraw this objection.

Under item V. 4., the Examiner submitted that the balance of the claims are obvious in view of various prior references. The Applicant notes that all of these claims incorporate the limitations of claim 1. As presented above, claim 1 is novel and non-obvious in view of the cited references, therefore, the Applicant submits that each claim reciting at least the same limitations would similarly be novel and non-obvious.

Therefore, the Application asks that the Examiner withdraw this objection under PCT Article 33(3).

With regard to item VII. 1., Applicant submits that the inclusion of reference numbers in the claims is not entirely appropriate as the figures do not correspond precisely with the elements of the claims. The Applicant submits that it would be confusing to make reference to the figures as requested.

With regard to item VII. 2., Applicant wishes to defer the amendment of the Background to the Invention until national entry applications have been filed.

The Applicant submits that he has complied with the requirements of item VII. 3., noting that the basis for the amendments to the claims is provided above.

With regard to item VIII. 1., the Applicant disagrees with the Examiner, submitting that the scope of claim 1 would be clear to one skilled in the art. As noted in Article 6, II-4.2 of the PCT Guidelines: "The claim should also be read with an attempt to make technical sense out of it".

With regard to item VIII. 2., the Applicant again disagrees with the Examiner, as the scope of claim 2 would also be clear to one skilled in the art. While an input signal *x(t)* may include spurious signals, noise, etc., it would be clear to the reader that an up-convertor would be designed with a particular purpose in mind, and that part of this design process would be the specification of the input and output signals involved.

The Applicant therefore asks that the Examiner withdraw these objections under PCT Article 6.

The Applicant believes that all of the objections levelled by the Examiner have now been addressed. The Applicant would be pleased to discuss any outstanding or new issues which may arise during preparation of a second Written Opinion, or the International Preliminary Examination Report.

for T. Gary O'Neill

Agent for the Applicant

TGO:MKL

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Two additional differences between the front end of the preferred embodiment of **Figure 6** and other embodiments described herein are:

- the generation of the DC offset signal for the summer **138** using the DSP **144** and a digital to analogue convertor (DAC) **150** (compare with the DC offset summer **104** and DC offset source **105** of **Figure 5**); and
- the addition of a third low pass filter LPF3I **146**, the de-aliasing filter for the analogue to digital convertor (ADC) **148** that follows. The design of this LPF3I **146** depends on the system specifications and design.

The design of the front end for the quadrature-phase of the input signal follows in the same manner, with components **152, 154, 156, 158, 160, 162, 164, 166** and **168** complementary to components **132, 134, 136, 138, 140, 142, 146, 148** and **150**, respectively. The input signals to these components are also quuadrature-phase complements to the in-phase signal inputs.

It is preferred to generate the inputs to the four mixers **132, 134, 152, 154** in the manner presented in **Figure 6**. Specifically, the φ_1I and φ_1Q generation block **170** generates signals φ_1I and φ_1Q, while φ_2I and φ_2Q generation block **172** generates signals φ_2I and φ_2Q. The input to these generation blocks **170, 172** is an oscillator which does not have a significant amount of signal power at the frequency of the RF signal. The construction of the necessary logic for these components would be clear to one skilled in the art from the description herein, and in particular, with reference to **Figure 3**. Such signals may be generated using basic logic gates, field programmable gate arrays (FPGA), read only memories (ROMs), micro-controllers or other devices known in the art. Further description and other means of generating such signals is presented in the co-pending patent application under the Patent Cooperation Treaty, Serial No. PCT/CA00/00996.

Note that the outputs of the φ_1I and φ_1Q generation block **170** go directly to mixers **132** and **152**, and also to the clocking edge delay and correction block **174** which corrects the φ_2I and φ_2Q signals. The clocking edge delay and correction block **174** also receives I and Q output control signals from the DSP **144**, which are digitized by DAC **176** and **178**, and are time corrected at blocks **180** and **182**. Correction blocks **180** and **182** modify the digitized signals from DAC **176** and **178** as required to suit the clocking edge delay and correction block **174**. There also may be a connection between the φ_1I and φ_1Q generation block **170** and the φ_2I and φ_2Q generation block **172** which may be required where φ_1I and φ_1Q are generated

10/070012
J[redacted]Rec'd PCT/PTO 28 FEB 2002

NEW CLAIMS

10/070012
JC13 Rec'd PCT/PTO 28 FEB 2002

WHAT IS CLAIMED IS:

1. A radio frequency (RF) down-convertor with reduced local oscillator leakage, for demodulating an input signal *x(t)*, comprising:
a synthesizer for generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;
a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said mixing signal φ_1 to generate an output signal *x(t)* φ_1; and
a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal *x(t)* φ_1 with said mixing signal φ_2 to generate an output signal *x(t)* φ_1 φ_2.

2. The radio frequency (RF) down-convertor of claim 1 wherein said synthesizer further comprises:
a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said input signal *x(t)* at baseband.

3. The radio frequency (RF) down-convertor of claim 2, further comprising:
a DC offset correction circuit.

4. The radio frequency (RF) down-convertor of claim 3, wherein said DC offset correction circuit comprises:
a DC source having a DC output; and
a summer for adding said DC output to an output of one of said mixers.

5. The radio frequency (RF) down-convertor of claim 2, further comprising:
a closed loop error correction circuit.

6. The radio frequency (RF) down-convertor of claim 5, wherein said closed loop error correction circuit further comprises:
an error level measurement circuit and
a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

7. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a power measurement.

8. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a voltage measurement.

9. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a current measurement.

10. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the phase delay of one of said mixing signals φ_1 and φ_2.

11. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the fall or rise time of one of said mixing signals φ_1 and φ_2.

12. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said mixing signals φ_1 and φ_2.

13. The radio frequency (RF) down-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where said mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

14. The radio frequency (RF) down-convertor of claim 1, further comprising:

a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

15. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are random.

16. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are pseudo-random.

17. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are irregular.

18. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are digital waveforms.

19. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are square waveforms.

20. The radio frequency (RF) down-convertor of claim 1, further comprising:
a local oscillator coupled to said synthesizer for providing a signal having a frequency that is an integral multiple of the desired mixing frequency.

21. The radio frequency (RF) down-convertor of claim 1, wherein said synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

22. The radio frequency (RF) down-convertor of claim 1, where said synthesizer uses different patterns to generate signals φ_1 and φ_2.

23. A method of demodulating a radio frequency (RF) signal $x(t)$ with reduced local oscillator leakage comprising the steps of:
generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;
mixing said input signal $x(t)$ with said mixing signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and
mixing said signal $x(t)\ \varphi_1$ with said mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

24. An integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 22.

25. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 22.

26. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 22.

COMPARE DOCUMENT

10/070012
Rec'd PCT/PTO 28 FEB 2002

WHAT IS CLAIMED IS:

1. A radio frequency (RF) down-convertor with reduced local oscillator leakage, for demodulating an input signal *x(t)*, comprising:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said ~~time-varying~~mixing signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal $x(t)\ \varphi_1$ with said ~~time-varying~~mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

2. The radio frequency (RF) down-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said input signal *x(t)* at baseband.

3. The radio frequency (RF) down-convertor of claim 2, further comprising:

a DC offset correction circuit.

4. The radio frequency (RF) down-convertor of claim 3, wherein said DC offset correction circuit comprises:

a DC source having a DC output; and

a summer for adding said DC output to an output of one of said mixers.

5. The radio frequency (RF) down-convertor of claim 2, further comprising:

a closed loop error correction circuit.

6. The radio frequency (RF) down-convertor of claim 5, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit and

a time-varying signal modification circuit for modifying a parameter of one of said ~~time-varying~~mixing signals φ_1 and φ_2 to minimize said error level.

7. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a power measurement.

8. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a voltage measurement.

9. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a current measurement.

10. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the phase delay of one of said ~~time-varying~~mixing signals φ_1 and φ_2.

11. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the fall or rise time of one of said ~~time-varying~~mixing signals φ_1 and φ_2.

12. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said ~~time-varying~~ mixing signals φ_1 and φ_2.

13. The radio frequency (RF) down-convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating ~~time-varying~~mixing signals φ_1 and φ_2, where said ~~time-varying~~mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

14. The radio frequency (RF) down-convertor of claim 1, further comprising:

a filter for removing unwanted signal components from said *x(t)* φ_1 signal.

15. The radio frequency (RF) down-convertor of claim ~~2~~1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are random.

16. The radio frequency (RF) down-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are pseudo-random.

17. The radio frequency (RF) down-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are irregular.

18. The radio frequency (RF) down-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are digital waveforms.

19. The radio frequency (RF) down-convertor of claim 1, wherein said ~~time-varying~~mixing signals φ_1 and φ_2 are square waveforms.

20. The radio frequency (RF) down-convertor of claim 1, further comprising:
a local oscillator coupled to said synthesizer for providing a signal having a frequency that is an integral multiple of the desired mixing frequency.

21. The radio frequency (RF) down-convertor of claim 1, wherein said synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

22. The radio frequency (RF) down-convertor of claim 1, where said synthesizer uses different patterns to generate signals φ_1 and φ_2.

2~~1~~3. A method of demodulating a radio frequency (RF) signal *x(t)* with reduced local oscillator leakage comprising the steps of:
generating ~~time-varying~~mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;
mixing said input signal *x(t)* with said ~~time-varying~~mixing signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and
mixing said signal $x(t)\ \varphi_1$ with said ~~time-varying~~mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

2~~2~~4. An integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 2~~0~~2.

2~~3~~5. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 2~~0~~2.

2~~4~~6. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 2~~0~~2.

PATENT COOPERATION TREATY

From the:
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

Gowling Lafleur Henderson LLP
Suite 2600
160 Elgin Street
Ottawa, Ontario K1P 1C3
CANADA

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WRITTEN OPINION

(PCT Rule 66)

Date of mailing *(day/month/year)*	17.07.2001	
Applicant's or agent's file reference O8-887954WO	**REPLY DUE**	**within 3 month(s)** from the above date of mailing
International application No. PCT/CA00/00994	International filing date *(day/month/year)* 01/09/2000	Priority date *(day/month/year)* 01/09/1999
International Patent Classification (IPC) or both national classification and IPC H04B1/04		
Applicant SiRiFIC WIRELESS CORPORATION et al.		

1. This written opinion is the **first** drawn up by this International Preliminary Examining Authority.

2. This opinion contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain document cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

3. The applicant is hereby **invited to reply** to this opinion.

   When? See the time limit indicated above. The applicant may, before the expiration of that time limit, request this Authority to grant an extension, see Rule 66.2(d).

   How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.

   Also: For an additional opportunity to submit amendments, see Rule 66.4. For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4 bis. For an informal communication with the examiner, see Rule 66.6.

   If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary examination report must be established according to Rule 69.2 is: 01/01/2002.

Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer / Examiner Kolbe, W
	Formalities officer (incl. extension of time limits) Kiepe, C Telephone No. +49 89 2399 2423

Form PCT/IPEA/408 (cover sheet) (January 1994)

I. Basis of the opinion

1. With regard to the **elements** of the international application (Replacement *sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed")*:

Description, pages:

1-16 as originally filed

Claims, No.:

1-24 as originally filed

Drawings, sheets:

1/8-8/8 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1,21
Inventive step (IS)	Claims	2-20,22-24
Industrial applicability (IA)	Claims	

2. Citations and explanations
   see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following documents:

   D1: WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11)
   D2: US-A-5 390 346 (D. MARZ) 14 February 1995 (1995-02-14)
   D3: GB-A-2 329 085 (GEC MARCONI) 10 March 1999 (1999-03-10)
   D4: EP-A-0 899 868 (MITEL CORP) 3 March 1999 (1999-03-03)

2. Document D1, see in particular the passages cited in the search report, discloses as in claim 1:

   A radio frequency (RF) down-convertor with reduced local oscillator leakage for demodulating an input signal x(t)(80 MHz R.F.) , comprising:
   a synthesizer for generating time-varying signals φ1 and φ2; where φ1*φ2 has significant power at the frequency (i.e. 81 MHz) of the local oscillator being emulated, and neither φ1 nor φ2 has significant power at the frequency of said local oscillator being emulated

   a first mixer (21) coupled to said synthesizer for mixing said input signal x(t) with said time varying signal φ1 to generat an output signal x(t) φ1; and

   a second mixer (26) coupled to said synthesizer and to the output of said first mixer for mixing said signal x(t) φ1 with said time varying signal φ2 to generat an output signal x(t) φ1 φ2

   The references in parentheses apply to the figures of D1.

   Since all the features of claim 1 are known from D1, the claim lacks novelty in the sense of Article 33(1),(2) PCT.

   It should be noted that any two stage mixer falls into the scope of claim 1, since

every local oscillator produces a "time-varying signal" because the voltage of such a signal varies in time with the frequency of the oscillator. The two conventional local oscillators of a double-superheterodyne stage emulate what the present application calls a "virtual local oscillator" whereby the sum or the difference of the frequencies of the two conventional local oscillators is considered the frequency of the "virtual local oscillator".

3. The subject-matter of independent claim 21 corresponds to the subject-matter of claim1, hence the above argumentation correspondingly applies to independent method claim 21.

4. Dependent claims 2 to 20 and 22 to 24 do not appear to contain any additional features which, in combination with the features of any claim to which they refer, involve an inventive step (Article 33(3) PCT) since these claims merely define an association of known features (see also D2 to D4) functioning in their normal way and, in combination, not producing any non-obvious working interrelationship, cf. PCT Guidelines Chapt. IV,8.8(B1).

<u>Re Item VII</u>

Certain defects in the international application

1. The features of the claims are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).

2. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1 to D3 is not mentioned in the description, nor are these documents identified therein.

3. If an amended set of claims is filed, then the description has to be adapted accordingly. The applicant is further requested to provide clear indication from where in the original application the amendments were derived, cf. Article 19(2) PCT.

Re Item VIII
Certain observations on the international application

1. Claim 1 tries to define the down-converter using parameters (the power at the frequency of a local oscillator being emulated) which are unsuitable to clearly define the structure of the down-convertor to be protected. Claim 1 is thus unclear in the sense of Article 6 PCT.

2. Claim 2 tries to define the convertor by reference to the input signal x(t) which may be applied to the a mixer of the convertor. Such a definition is unsuitable to clearly define the structure of the claimed convertor. This claims is thus unclear, Article 6 PCT.

PATENT COOPERATION TREATY

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From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

Gowling Lafleur Henderson LLP
Suite 2600
160 Elgin Street
Ottawa, Ontario K1P 1C3
CANADA

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of mailing *(day/month/year)* 17.01.2002

Applicant's or agent's file reference O8-887954WO	**IMPORTANT NOTIFICATION**	
International application No. PCT/CA00/00994	International filing date *(day/month/year)* 01/09/2000	Priority date *(day/month/year)* 01/09/1999
Applicant SiRiFIC WIRELESS CORPORATION et al.		

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

   The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

   Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

   For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/ European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Teschauer, B Tel.+49 89 2399-8231

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PATENT COOPERATION TREATY

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PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

12

Applicant's or agent's file reference O8-887954WO	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/CA00/00994	International filing date *(day/month/year)* 01/09/2000	Priority date *(day/month/year)* 01/09/1999
International Patent Classification (IPC) or national classification and IPC H04B1/04		
Applicant SiRiFIC WIRELESS CORPORATION et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 5 sheets.

3. This report contains indications relating to the following items:

   I ☒ Basis of the report
   II ☐ Priority
   III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   IV ☐ Lack of unity of invention
   V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   VI ☐ Certain documents cited
   VII ☒ Certain defects in the international application
   VIII ☒ Certain observations on the international application

Date of submission of the demand 29/03/2001	Date of completion of this report 17.01.2002
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Kolbe, W Telephone No. +49 89 2399 8479

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, pages:

1-13,15,16	as originally filed			
14	as received on	17/12/2001	with letter of	17/12/2001

Claims, No.:

1-26	as received on	17/12/2001	with letter of	17/12/2001

Drawings, sheets:

1/8-8/8	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	2-22,24-26
	No:	Claims	1,23
Inventive step (IS)	Yes:	Claims	
	No:	Claims	2-22,24-26
Industrial applicability (IA)	Yes:	Claims	1-26
	No:	Claims	

2. Citations and explanations
   see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following documents:

   D1: WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11)
   D2: US-A-5 390 346 (D. MARZ) 14 February 1995 (1995-02-14)
   D3: GB-A-2 329 085 (GEC MARCONI) 10 March 1999 (1999-03-10)
   D4: EP-A-0 899 868 (MITEL CORP) 3 March 1999 (1999-03-03)

2. Document D1, see in particular the passages cited in the search report, discloses as in claim 1:

   A radio frequency (RF) down-convertor with reduced local oscillator leakage for demodulating an input signal x(t)(80 MHz R.F.) , comprising:

   a synthesizer (22,24,27,28) for generating mixing signals φ1 and φ2 which vary irregularly over time (since the are spreaded); where φ1*φ2 has significant power at the frequency (i.e. 81 MHz) of the local oscillator being emulated, and neither φ1 nor φ2 has significant power at the frequency of said local oscillator being emulated (even though the signals φ1 and φ2 are spread they do not have significant energy at 81 MHz)

   a first mixer (21) coupled to said synthesizer for mixing said input signal x(t) with said mixing signal φ1 to generate an output signal x(t) φ1 (any mixer generates an output signal composed from the product of its input signals) ; and

   a second mixer (26) coupled to said synthesizer and to the output of said first mixer for mixing said signal x(t) φ1 with said mixing signal φ2 to generate an output signal x(t) φ1 φ2 (again, any mixer generates an output signal composed from the product of its input signals)

   The references in parentheses apply to the figures of D1.

It should be noted that the structure claimed by claim 1 is identical to the structure disclosed by D1 in its claim 1 which does not provide any additional filters.

Since all the features of claim 1 are known from D1, the claim lacks novelty in the sense of Article 33(1),(2) PCT.

3. The subject-matter of independent claim 23 corresponds to the subject-matter of claim 1, hence the above argumentation correspondingly applies to independent method claim 23.

4. Dependent claims 2 to 23 and 24 to 26 do not contain any additional features which, in combination with the features of any claim to which they refer, involve an inventive step (Article 33(3) PCT) since these claims merely define an association of known features (see also D2 to D4) functioning in their normal way and, in combination, not producing any non-obvious working interrelationship, cf. PCT Guidelines Chapt. IV,8.8(B1).

Re Item VII

Certain defects in the international application

1. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1 to D3 is not mentioned in the description, nor are these documents identified therein.

Re Item VIII

Certain observations on the international application

1. Claim 1 tries to define the down-converter using parameters (the power at the frequency of a local oscillator being emulated) which are unsuitable to clearly define the structure of the down-convertor to be protected. Claim 1 is thus unclear in the sense of Article 6 PCT.

2. Claim 2 tries to define the convertor by reference to the input signal x(t) which may be applied to the a mixer of the convertor. Such a definition is unsuitable to clearly define the structure of the claimed convertor. This claims is thus unclear,

Article 6 PCT.

Two additional differences between the front end of the preferred embodiment of **Figure 6** and other embodiments described herein are:

- the generation of the DC offset signal for the summer **138** using the DSP **144** and a digital to analogue convertor (DAC) **150** (compare with the DC offset summer **104** and DC offset source **105** of **Figure 5**); and
- the addition of a third low pass filter LPF3I **146**, the de-aliasing filter for the analogue to digital convertor (ADC) **148** that follows. The design of this LPF3I **146** depends on the system specifications and design.

The design of the front end for the quadrature-phase of the input signal follows in the same manner, with components **152, 154, 156, 158, 160, 162, 164, 166** and **168** complementary to components **132, 134, 136, 138, 140, 142, 146, 148** and **150**, respectively. The input signals to these components are also quuadrature-phase complements to the in-phase signal inputs.

It is preferred to generate the inputs to the four mixers **132, 134, 152, 154** in the manner presented in **Figure 6**. Specifically, the φ_1I and φ_1Q generation block **170** generates signals φ_1I and φ_1Q, while φ_2I and φ_2Q generation block **172** generates signals φ_2I and φ_2Q. The input to these generation blocks **170, 172** is an oscillator which does not have a significant amount of signal power at the frequency of the RF signal. The construction of the necessary logic for these components would be clear to one skilled in the art from the description herein, and in particular, with reference to **Figure 3**. Such signals may be generated using basic logic gates, field programmable gate arrays (FPGA), read only memories (ROMs), micro-controllers or other devices known in the art. Further description and other means of generating such signals is presented in the co-pending patent application under the Patent Cooperation Treaty, Serial No. PCT/CA00/00996.

Note that the outputs of the φ_1I and φ_1Q generation block **170** go directly to mixers **132** and **152**, and also to the clocking edge delay and correction block **174** which corrects the φ_2I and φ_2Q signals. The clocking edge delay and correction block **174** also receives I and Q output control signals from the DSP **144**, which are digitized by DAC **176** and **178**, and are time corrected at blocks **180** and **182**. Correction blocks **180** and **182** modify the digitized signals from DAC **176** and **178** as required to suit the clocking edge delay and correction block **174**. There also may be a connection between the φ_1I and φ_1Q generation block **170** and the φ_2I and φ_2Q generation block **172** which may be required where φ_1I and φ_1Q are generated

WHAT IS CLAIMED IS:

1. A radio frequency (RF) down-convertor with reduced local oscillator leakage, for demodulating an input signal *x(t)*, comprising:

a synthesizer for generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said mixing signal φ_1 to generate an output signal *x(t)* φ_1; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal *x(t)* φ_1 with said mixing signal φ_2 to generate an output signal *x(t)* φ_1 φ_2.

2. The radio frequency (RF) down-convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said input signal *x(t)* at baseband.

3. The radio frequency (RF) down-convertor of claim 2, further comprising:

a DC offset correction circuit.

4. The radio frequency (RF) down-convertor of claim 3, wherein said DC offset correction circuit comprises:

a DC source having a DC output; and

a summer for adding said DC output to an output of one of said mixers.

5. The radio frequency (RF) down-convertor of claim 2, further comprising:

a closed loop error correction circuit.

6. The radio frequency (RF) down-convertor of claim 5, wherein said closed loop error correction circuit further comprises:

an error level measurement circuit and

a time-varying signal modification circuit for modifying a parameter of one of said mixing signals φ_1 and φ_2 to minimize said error level.

7. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a power measurement.

8. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a voltage measurement.

9. The radio frequency (RF) down-convertor of claim 6, wherein said error level measurement circuit comprises a current measurement.

10. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the phase delay of one of said mixing signals φ_1 and φ_2.

11. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter is the fall or rise time of one of said mixing signals φ_1 and φ_2.

12. The radio frequency (RF) down-convertor of claim 6, wherein said modified parameter includes both the phase delay and the fall or rise time of one of said mixing signals φ_1 and φ_2.

13. The radio frequency (RF) down-convertor of claim 2 wherein said synthesizer further comprises:
a synthesizer for generating mixing signals φ_1 and φ_2, where said mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

14. The radio frequency (RF) down-convertor of claim 1, further comprising:
a filter for removing unwanted signal components from said $x(t)$ φ_1 signal.

15. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are random.

16. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are pseudo-random.

17. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are irregular.

18. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are digital waveforms.

19. The radio frequency (RF) down-convertor of claim 1, wherein said mixing signals φ_1 and φ_2 are square waveforms.

20. The radio frequency (RF) down-convertor of claim 1, further comprising:
a local oscillator coupled to said synthesizer for providing a signal having a frequency that is an integral multiple of the desired mixing frequency.

21. The radio frequency (RF) down-convertor of claim 1, wherein said synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

22. The radio frequency (RF) down-convertor of claim 1, where said synthesizer uses different patterns to generate signals φ_1 and φ_2.

23. A method of demodulating a radio frequency (RF) signal *x(t)* with reduced local oscillator leakage comprising the steps of:
generating mixing signals φ_1 and φ_2 which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated;
mixing said input signal *x(t)* with said mixing signal φ_1 to generate an output signal *x(t)* φ_1; and
mixing said signal *x(t)* φ_1 with said mixing signal φ_2 to generate an output signal *x(t)* $\varphi_1\,\varphi_2$.

24. An integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 22.

25. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 22.

26. A computer data signal embodied in a carrier wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio frequency (RF) down-convertor of any one of claims 1 - 22.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
08-887954WO		
International application No. PCT/CA 00/00994	International filing date *(day/month/year)* 01/09/2000	(Earliest) Priority Date *(day/month/year)* 01/09/1999
Applicant SiRiFIC WIRELESS CORPORATION et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.
      [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).
   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :
      [ ] contained in the international application in written form.
      [ ] filed together with the international application in computer readable form.
      [ ] furnished subsequently to this Authority in written form.
      [ ] furnished subsequently to this Authority in computer readble form.
      [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
      [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished
2. [ ] **Certain claims were found unsearchable** (See Box I).
3. [ ] **Unity of invention is lacking** (see Box II).
4. With regard to the **title,**
   [ ] the text is approved as submitted by the applicant.
   [X] the text has been established by this Authority to read as follows:
   FREQUENCY TRANSLATOR USING A NON-PERIODIC LOCAL OSCILLATOR SIGNAL
5. With regard to the **abstract,**
   [X] the text is approved as submitted by the applicant.
   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. The figure of the **drawings** to be published with the abstract is Figure No. 3
   [X] as suggested by the applicant.
   [ ] because the applicant failed to suggest a figure.
   [ ] because this figure better characterizes the invention.
   [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/CA 00/00994

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/04 H03D7/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11) page 2, line 18 -page 3, line 25 page 4, line 5 -page 5, line 32; figure 2	1,2, 13-24
X	US 5 390 346 A (D. MARZ) 14 February 1995 (1995-02-14) column 4, line 34 -column 5, line 60; figure 1	1,2,13, 14,20-24
A	GB 2 329 085 A (GEC MARCONI) 10 March 1999 (1999-03-10) page 5, line 6 -page 11, line 5; figures 1,2 claims 1,2; figure 3	3,4
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 February 2001	20/02/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Butler, N

1

Form PCT/ISA/210 (second sheet) (July 1992)

International Application No
PCT/CA 00/00994

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 899 868 A (MITEL CORP) 3 March 1999 (1999-03-03) column 1, line 22 - line 42; figures 1,2 claims 1-6 -----	1-24

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/CA 00/00994

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9601006 A	11-01-1996	AU 2909795 A	25-01-1996
US 5390346 A	14-02-1995	NONE	
GB 2329085 A	10-03-1999	AU 9083698 A WO 9913590 A	29-03-1999 18-03-1999
EP 0899868 A	03-03-1999	CA 2245958 A	28-02-1999